IN THE CLAIMS

What is claimed is:

1. A monitoring structure, comprising:

at least one monitoring trench formed through a first layer and terminating at a second layer; and

a feature formed in, with, or in relation to the monitoring trench that are configured to monitor at least one process step that forms corresponding features in, with, or in relation to non-monitoring trenches in a different layer than the first layer.

2. The monitoring structure of claim 1, wherein:

the first layer includes a deposited layer of a predetermined thickness.

3. The monitoring structure of claim 1, wherein:

the first layer comprises polysilicon; and

the different layer comprises an essentially monocrystalline silicon wafer substrate.

4. The monitoring structure of claim 1, wherein:

the first layer comprises silicon formed over a non-semiconductor-on-insulator (SOI) wafer substrate; and

the different layer comprises a silicon layer formed over a substrate insulating

layer on a SOI wafer substrate.

5. The monitoring structure of claim 1, wherein:

the second layer comprises silicon dioxide.

6. The monitoring structure of claim 1, wherein:

the second layer comprises an etch stop layer and forms a bottom of the at least one monitor trench.

7. The monitoring structure of claim 1, wherein:

the trenches formed in a different layer are shallow trench isolation (STI) structures formed in an integrated circuit substrate; and

the at least one step includes a planarization step and the feature includes a step height of a STI insulator material.

8. The monitoring structure of claim 7, wherein:

the planarization step includes chemical-mechanical polishing.

9. The monitoring structure of claim 1, wherein:

the trenches formed in a different layer are lateral island isolation regions in a semiconductor-on-insulator substrate.

10. A method of forming a monitoring structure, comprising the steps of:

etching a first layer to form monitor trenches that extend through the first layer and stop at an etch stop layer on a monitor wafer; and

forming a feature in, with, or in relation to the monitor trenches, wherein a process to be monitored with said monitor structure forms a corresponding non-monitor trench in a different layer or material than the first layer.

11. The method of claim 10, further including:

the feature can vary according to a different trench depth; and

depositing a first layer to a predetermined thickness equivalent to a desired trench depth.

12. The method of claim 11, further including:

forming an etch stop layer comprising silicon dioxide on a semiconductor substrate; and

depositing the first layer includes depositing a layer comprising polysilicon having a thickness less than 5000 angstroms.

13. The method of claim 10, further including:

the monitor wafer is a non semiconductor-on-insulator (SOI) wafer and the normal wafer is a SOI wafer having semiconductor islands of a predetermined thickness; and

depositing a first layer of the predetermined thickness.

14. The method of claim 10, wherein:

etching the first layer includes forming a substrate trench etch mask on the first layer.

15. The method of claim 10, wherein:

etching the first layer includes forming a substrate trench etch mask pattern that essentially matches a semiconductor-on-insulator wafer lateral island isolation pattern.

16. The method of claim 10, wherein:

etching the first layer includes substantially anisotropically etching with a selectivity between the first layer and the second layer of greater than 30:1.

17. The method of claim 10, wherein:

forming a feature includes planarizing a trench insulator material that extends inside the monitor trenches.

18. The method of claim 17, wherein:

planarizing includes chemical-mechanical polishing the trench insulator material.

19. The method of claim 10, wherein:

forming a feature includes forming a feature selected from the group consisting of at least a portion of a semiconductor-on-insulator (SOI) transistor, SOI contact, and SOI interlayer dielectric.

20. A method of monitoring a semiconductor manufacturing process, comprising the steps of:

processing a monitor wafer having monitoring trenches formed in a first layer of the monitoring wafer according to at least one process step that forms a feature, the feature being formed in a non-monitoring wafer in, with, or in relation to a different layer than the first layer in the semiconductor manufacturing process.

21. The method of claim 20, wherein:

the first layer comprises a deposited layer and the different layer comprises a wafer substrate.

22. The method of claim 20, wherein:

the first layer comprises a deposited layer and the different layer comprises a semiconductor island layer formed over a semiconductor-on-insulator wafer substrate.

23. The method of claim 20, wherein:

the at least one process step includes depositing and planarizing a trench insulating material.

24. The method of claim 20, further including:

running the monitor wafer through the at least one process step with at

least one normal wafer.

25. The method of claim 20, further including:

the features include a trench insulator step height; and

examining the monitor structure in cross section to measure the insulator step height.

26. The method of claim 25, wherein:

the at least one process step include a shallow trench isolation (STI) insulator deposition step and a STI insulator chemical-mechanical polishing step.